



3N90Z

Preliminary

Power MOSFET

3 Amps, 900 Volts N-CHANNEL POWER MOSFET

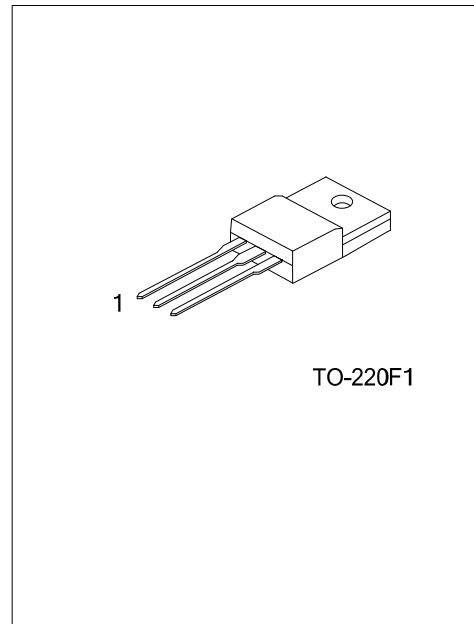
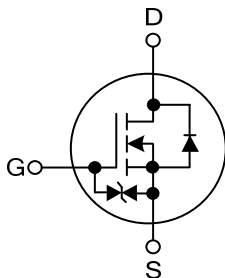
DESCRIPTION

The UTC **3N90Z** provides excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

- * $R_{DS(ON)}=4.1\Omega @V_{GS}=10\text{ V}$
- * Ultra Low Gate Charge (typical 22.7 nC)
- * Low Reverse Transfer Capacitance (C_{RSS} = Typical 13 pF)
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
3N90ZL-TF1-T	3N90ZG-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>3N90ZL-TF1-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TF1: TO-220F1</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage ($V_{GS}=0\text{V}$)	V_{DSS}	900	V
Drain-Gate Voltage ($R_G=20\text{k}\Omega$)	V_{DGR}	900	V
Gate-Source Voltage	V_{GSS}	± 20	V
Gate-Source Breakdown Voltage ($I_{GS}=\pm 1\text{mA}$)	BV_{GSO}	30(MIN)	V
Insulation Withstand Voltage (DC)	V_{ISO}	2500	V
Avalanche Current (Note 2)	I_{AR}	3	A
Continuous Drain Current	I_D	3	A
Pulsed Drain Current	I_{DM}	10	A
Single Pulse Avalanche Energy (Note 3)	E_{AS}	180	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation	P_D	25	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by $T_{J(MAX)}$

3. starting $T_J=25^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{V}$

4. $I_{SD} \leq 3\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq T_{J(MAX)}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	5	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	900			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=900V, V_{GS}=0V$			1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	3.75	4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1.5A$		4.1	4.8	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$		590		pF
Output Capacitance	C_{OSS}			63		pF
Reverse Transfer Capacitance	C_{RSS}			13		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=450V, I_D=1.5A, R_G=4.7\Omega$		18		ns
Turn-On Rise Time	t_R	$V_{GS}=10V$		7		ns
Turn-Off Delay Time	$t_{D(OFF)}$	$V_{DD}=720V, I_D=1.5A, R_G=4.7\Omega$		45		ns
Turn-Off Fall Time	t_F	$V_{GS}=10V$		18		ns
Total Gate Charge	Q_G	$V_{DD}=720V, I_D=3A, V_{GS}=10V$		22.7		nC
Gate-Source Charge	Q_{GS}			4.2		nC
Gate-Drain Charge	Q_{DD}			12		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage(Note 1)	V_{SD}	$I_{SD}=3A, V_{GS}=0V$			1.6	V
Source-Drain Current	I_{SD}				3	A
Source-Drain Current (Pulsed)	I_{SDM}				12	A
Reverse Recovery Current	I_{RRM}	$I_{SD}=3A, di/dt=100A/\mu s, V_{DD}=100V, T_J=25^\circ\text{C}$		8.7		A
Body Diode Reverse Recovery Time	t_{RR}			510		ns
Body Diode Reverse Recovery Charge	Q_{RR}			2.2		nC

Notes: 1. Pulse width=300 μs , Duty cycle $\leq 1.5\%$

2. $C_{OSS(EQ)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

■ TEST CIRCUITS AND WAVEFORMS

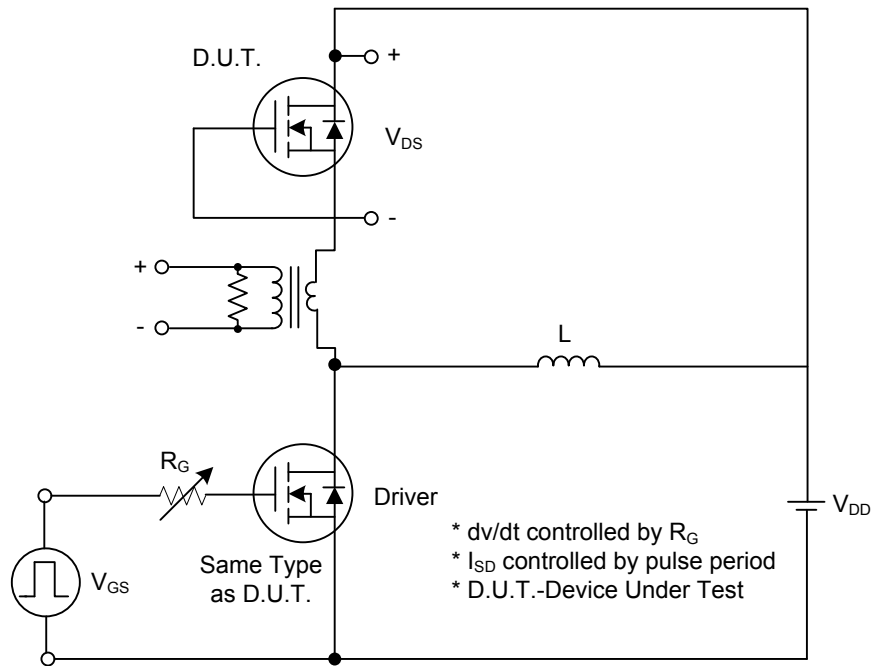


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

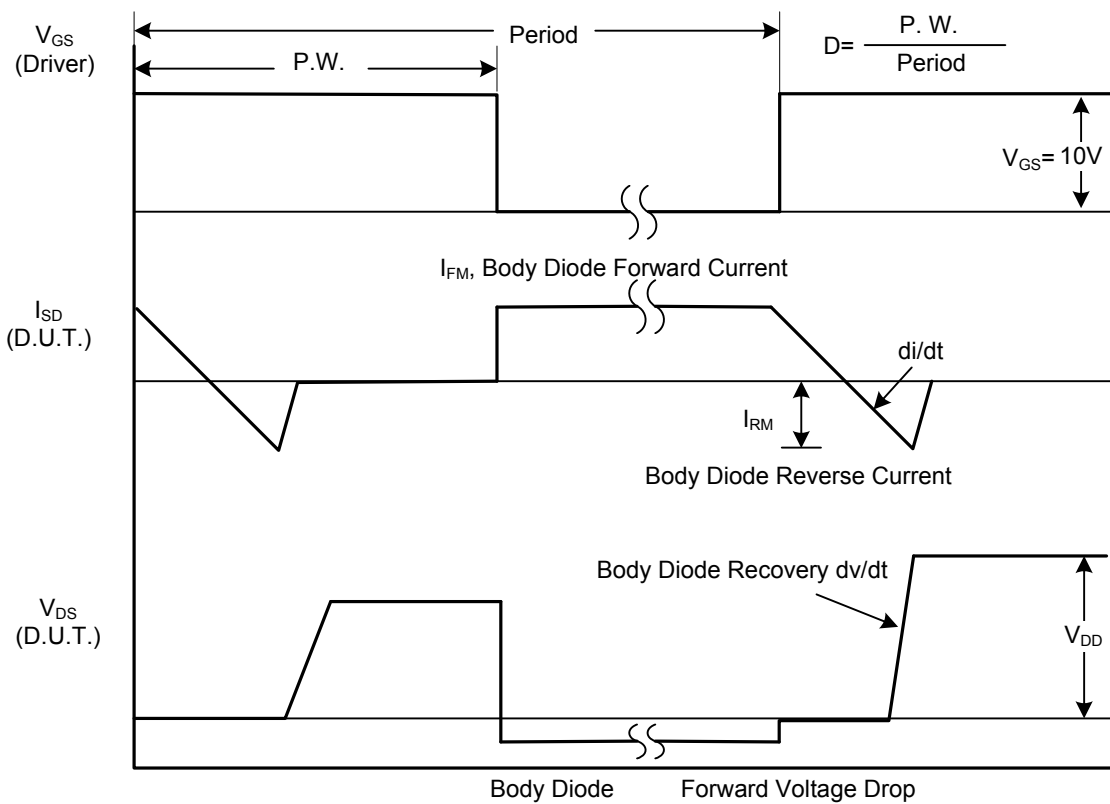


Fig. 1B Peak Diode Recovery dv/dt Waveforms

TEST CIRCUITS AND WAVEFORMS (Cont.)

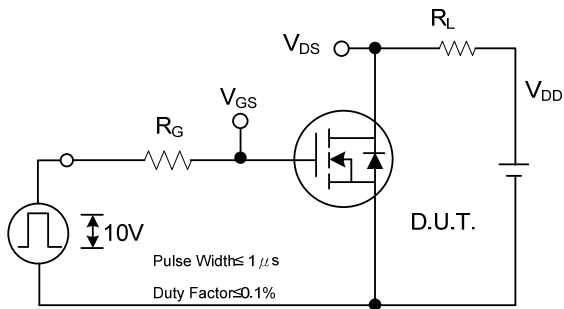


Fig. 2A Switching Test Circuit

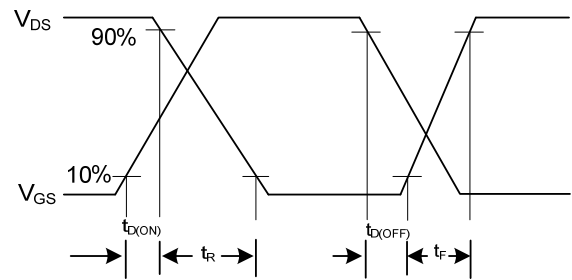


Fig. 2B Switching Waveforms

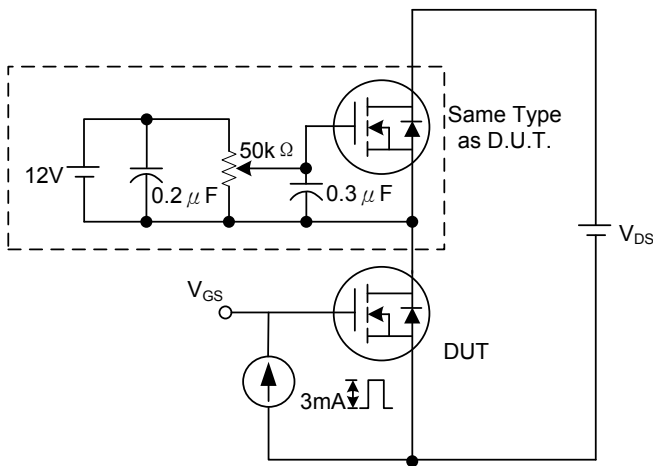


Fig. 3A Gate Charge Test Circuit

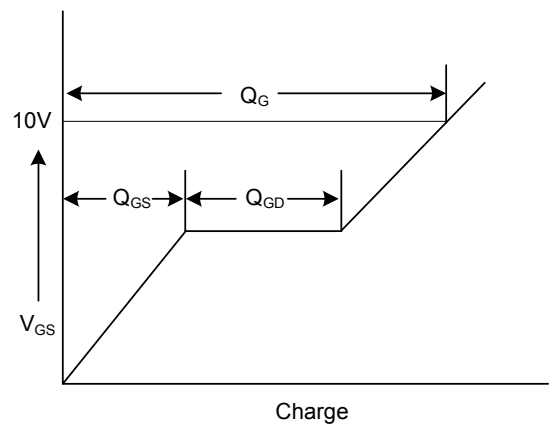


Fig. 3B Gate Charge Waveform

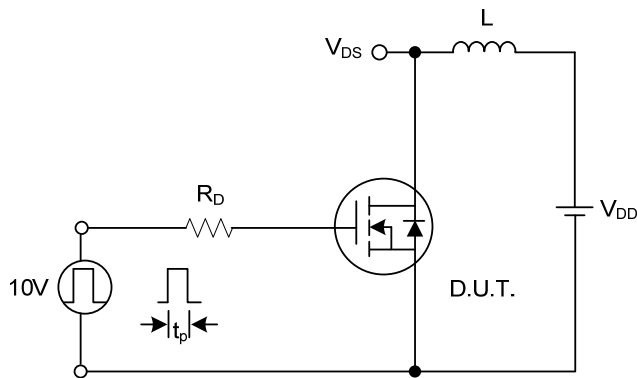


Fig. 4A Unclamped Inductive Switching Test Circuit

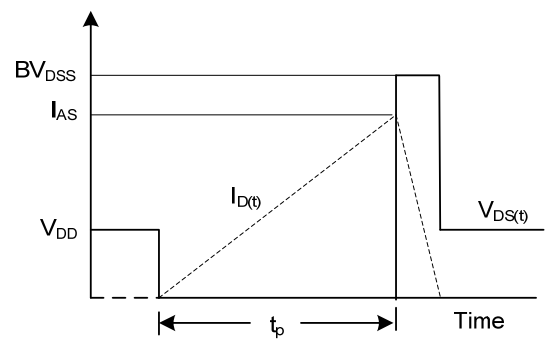


Fig. 4B Unclamped Inductive Switching Waveforms

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